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RESPONSE UNDER 37 C.F.R. § 1.116  
EXPEDITING PROCEDURE  
EXAMINING GROUP 2800

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Low, *et al.* Docket No.: 02 P 15173 US / INTECH  
3.0-076  
Serial No.: 10/689,233 Art Unit: 2891  
Filed: October 20, 2003 Examiner: Asok K. Sarkar  
For: Inclusion Of Low-K Dielectric Material Between Bit Lines

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AICS  
3/10/06

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**RESPONSE UNDER 37 C.F.R. § 1.116**

Dear Sir:

The following remarks are presented in response to the Examiner's Final Office Action  
mailed December 28, 2005.